LISTING OF THE CLAIMS:

Claims 1-52 (Previously Canceled)

53. (Currently Amended) A dual workfunction high-performance support MOSFET/EDRAM array comprising at least one support region and at least one array region, said array region and said support region being separated by an isolation region, and at least a gate conductor guard ring formed around said array region on top of said isolation region, wherein said gate conductor guard ring prevents trapping of a stringer of gate conductor polysilicon on said isolation region.

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54. (Original) The dual workfunction high-performance support MOSFET/EDRAM array of Claim 53 wherein said array region includes a plurality of DRAM cells embedded in a semiconductor substrate.

55. (Original) The dual workfunction high-performance support MOSFET/EDRAM array of Claim 54 wherein wordlines overlay each of said DRAM cells and a bitline overlays said wordlines.

56. (Original) The dual workfunction high-performance support MOSFET/EDRAM array of Claim 54 wherein each of said DRAM cells are vertical DRAMs.

57. (Original) A dual workfunction high-performance support MOSFET/EDRAM array comprising at least one support region having a local interconnect formed therein and at least one array region having at least one wordline formed therein, said at least one array

region and said at least one support region are separated by an isolation region, and said at least one wordline and said local interconnect are comprised of identical material.

58. (Original) The dual workfunction high-performance support MOSFET/EDRAM array of Claim 57 wherein said at least one array region includes a plurality of DRAM cells embedded in a semiconductor substrate.

59. (Original) The dual workfunction high-performance support MOSFET/EDRAM array of Claim 58 wherein said DRAM cells are vertical DRAMs.